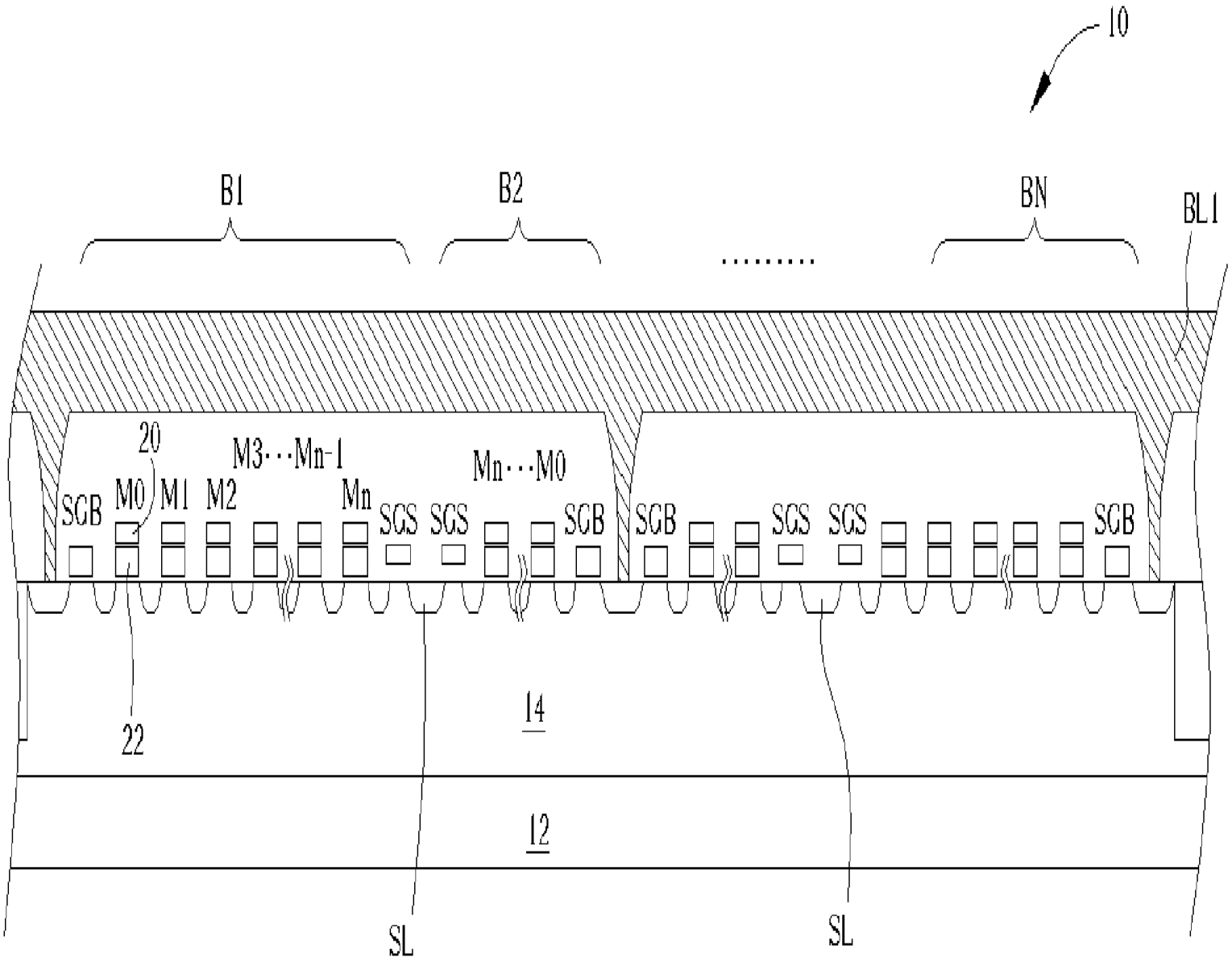


Fig. 1 Prior art

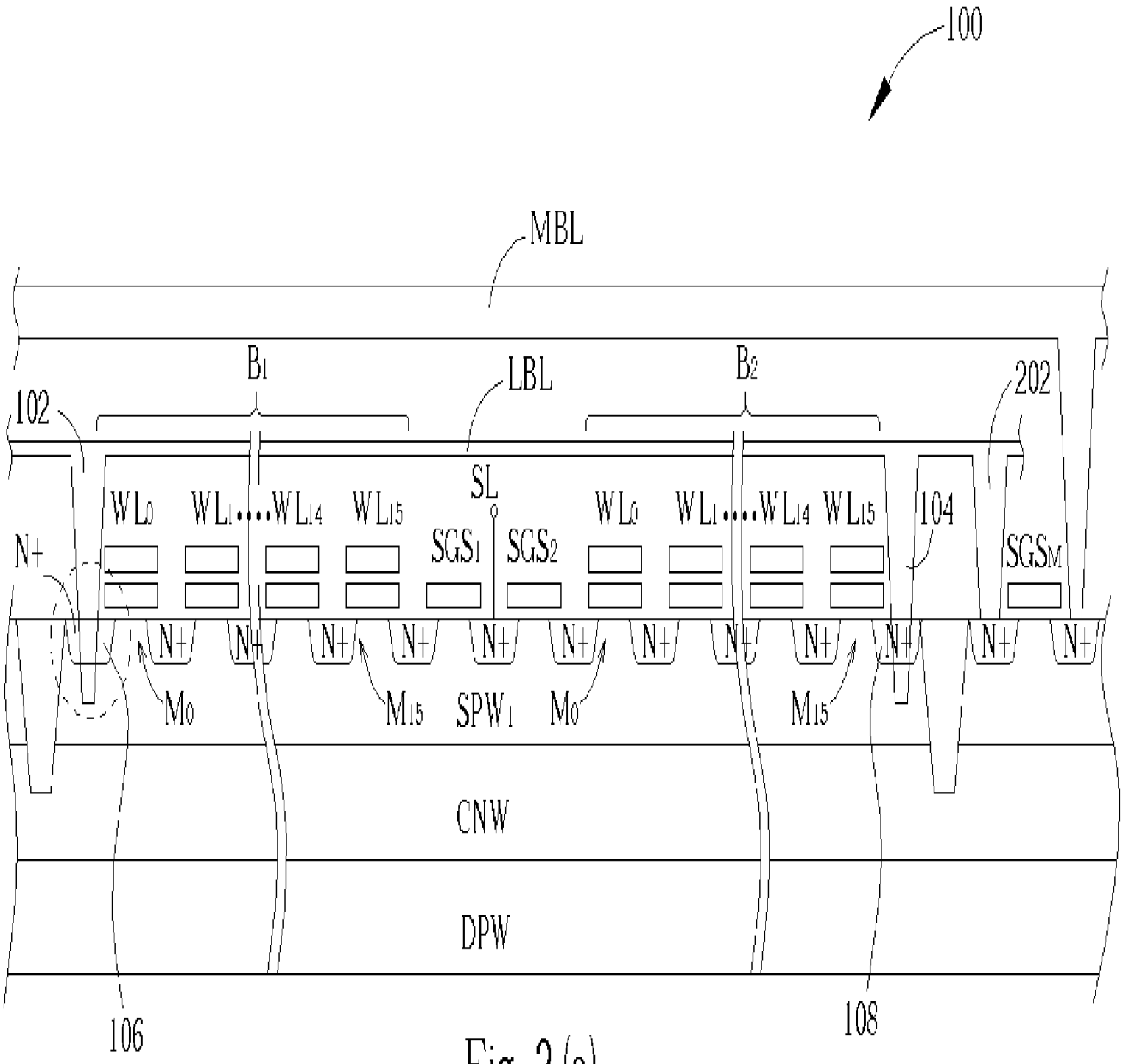
100
MBL
B1
LBL
B2
202
102
SL
WL0
WL1
WL14
WL15
SGS1
SGS2
WL0
WL1
WL14
WL15
104
SGSM
N+
M0
M15
SPW1
M0
M15
CNW
DPW
106
108

Fig. 2 (a)

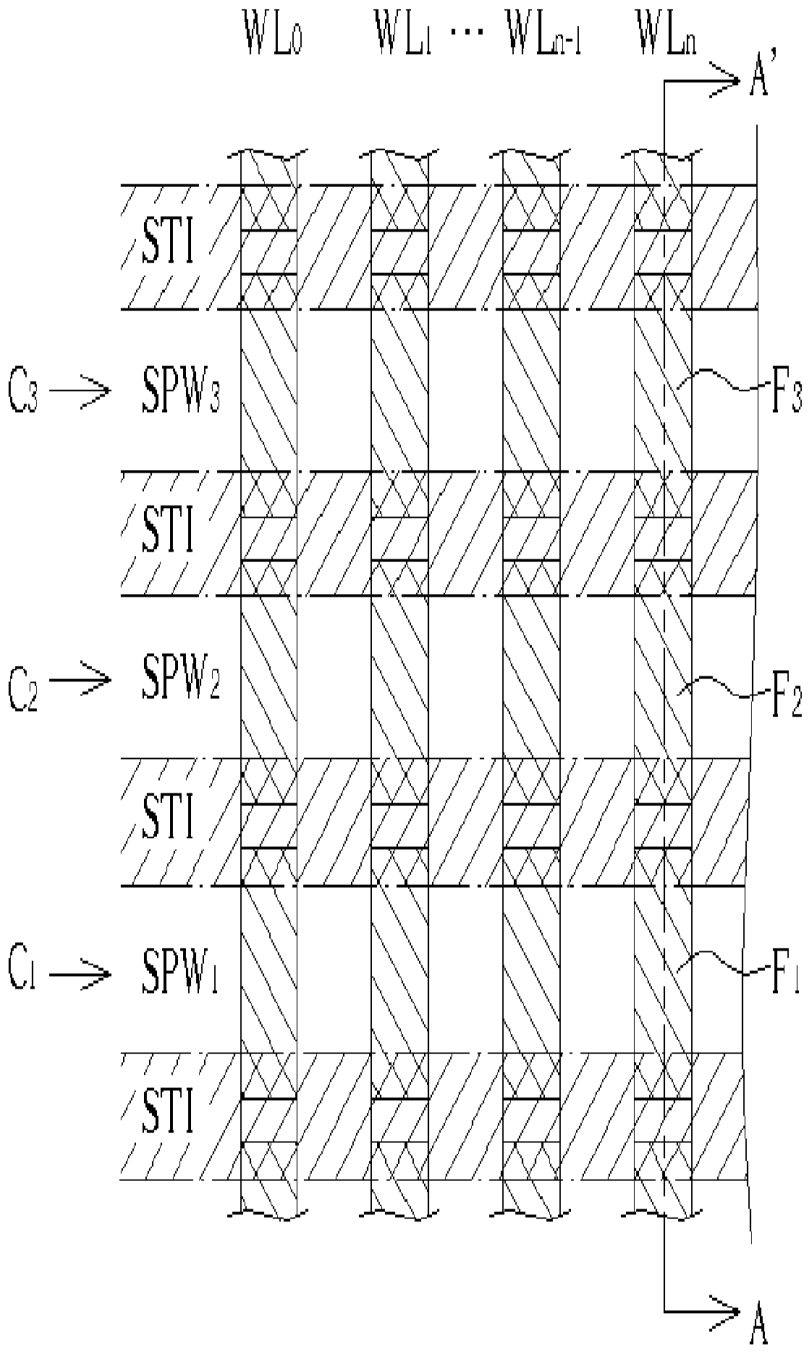
WL0
WL1 ··· WLn-1
WLn
A'
STI
C3
SPW3
F3
STI
C2
SPW2
F2
STI
C1
SPW1
F1
STI
A

Fig. 2 (b)

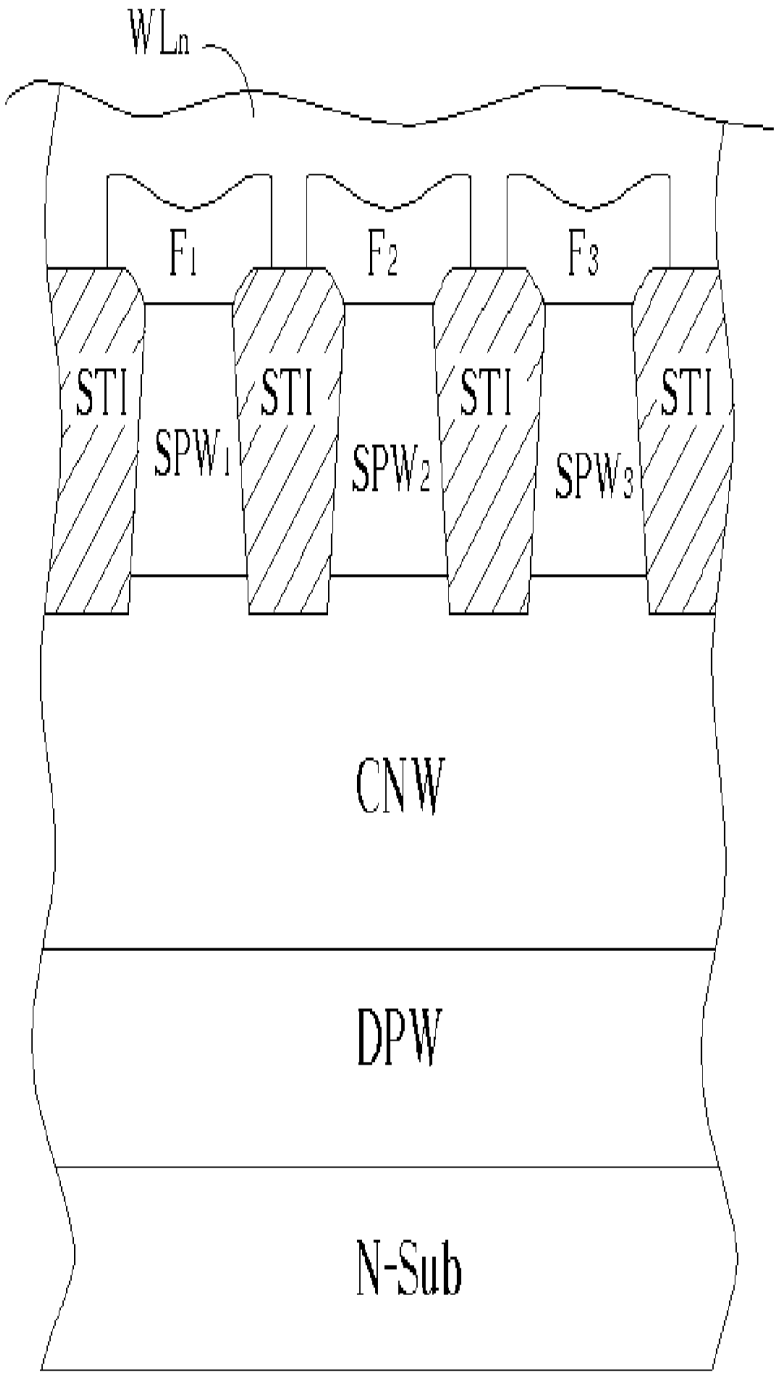


Fig. 2 (c)

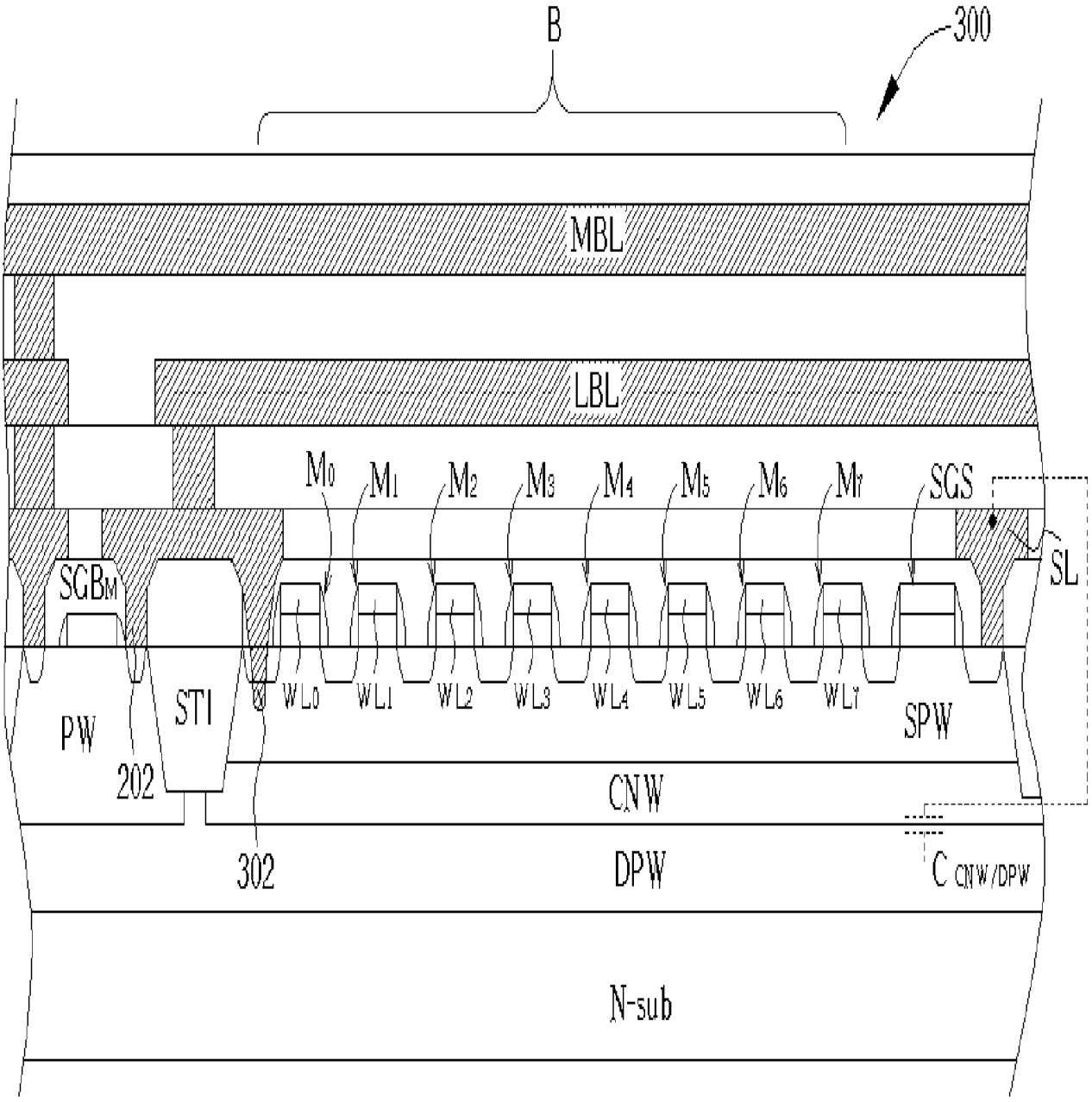
B
300
MBL
LBL
M0
M1
M2
M3
M4
M5
M6
M7
SGS
SL
SGBM
PW
STI
202
302
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
SPW
CNW
DPW
C CNW/DPW
N-sub

Fig. 3 (a)

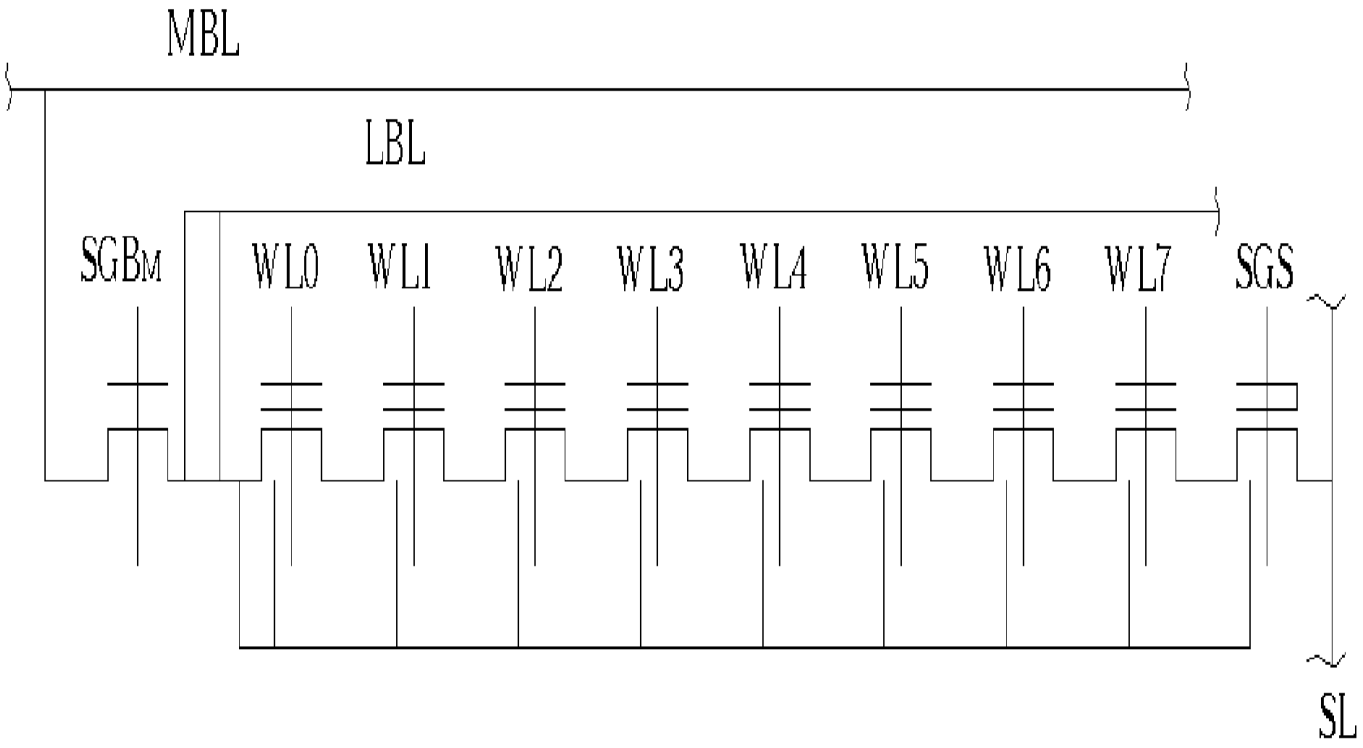


Fig. 3 (b)

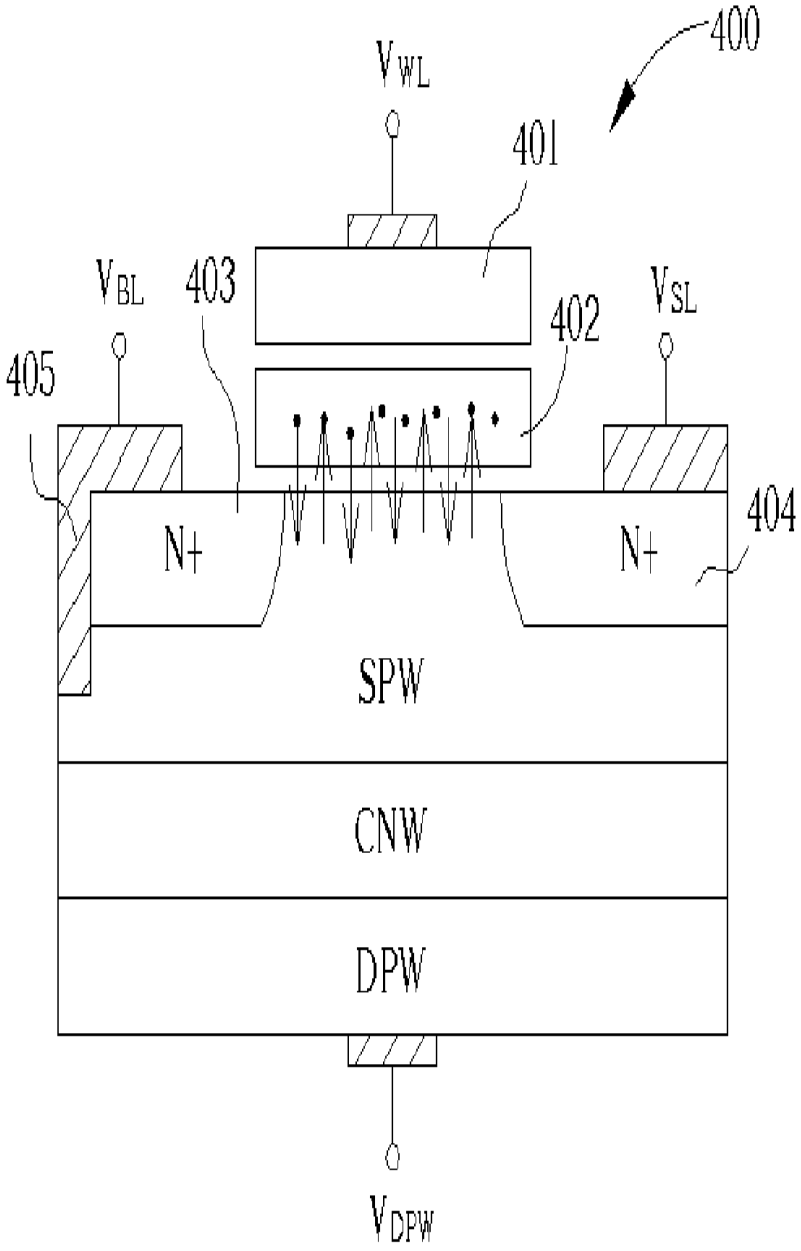


Fig. 4 (a)

| | $V_{BL}$ | $V_{WL}$ | $V_{SL}$ | $V_{DPW}$ |
|---|---|---|---|---|
| Program | 5V | -10V | Float | 0V |
| Erase | Float | 10V | -8V | -8V |
| Read | 0V | 0V | 1.5V | 0V |

Fig. 4 (b)

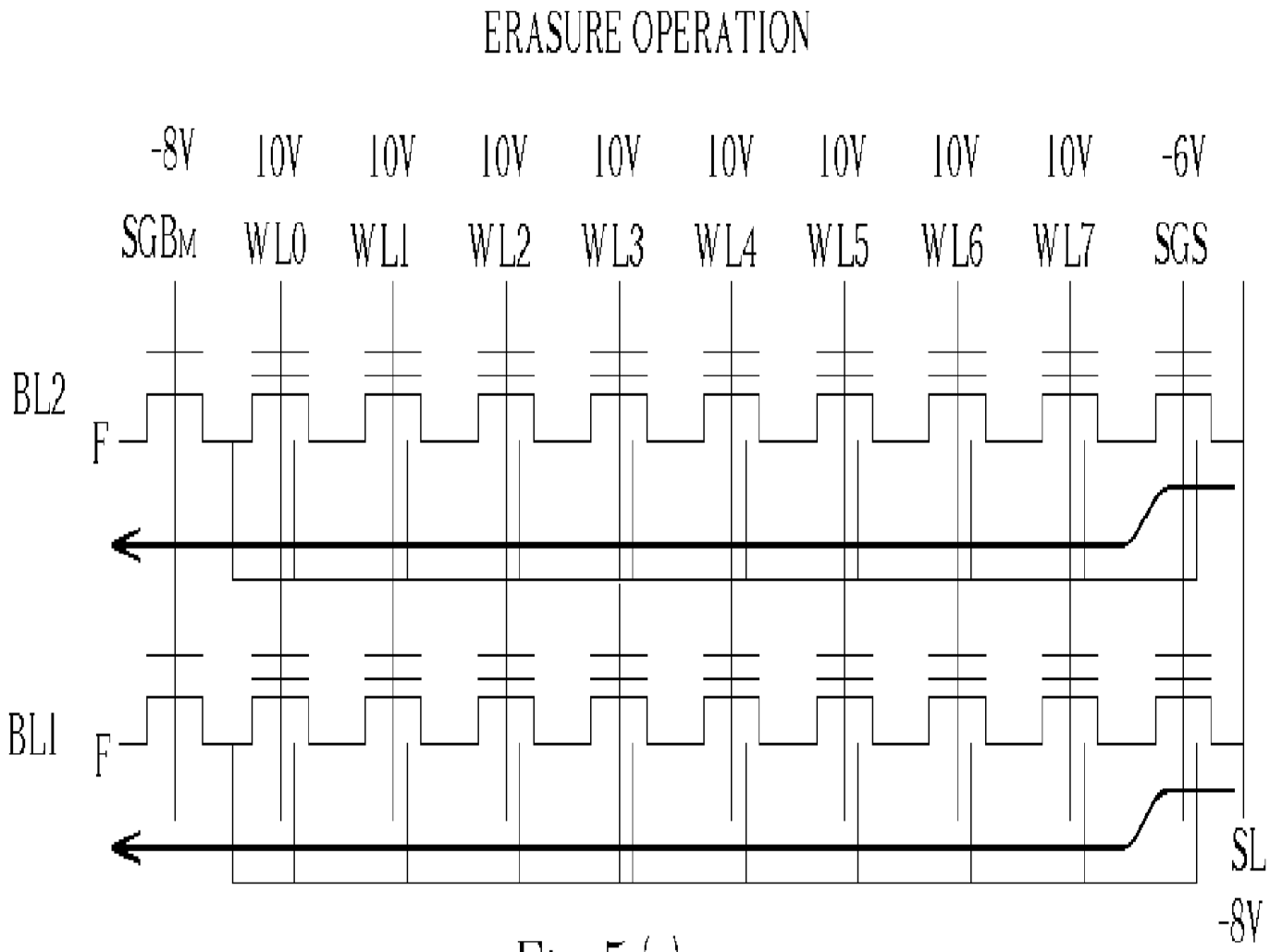
ERASURE OPERATION
-8V
10V
10V
10V
10V
10V
10V
10V
10V
-6V
SGBM
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
SGS
BL2
F
BL1
F
SL
-8V

Fig. 5 (a)

PROGRAMMING OPERATION

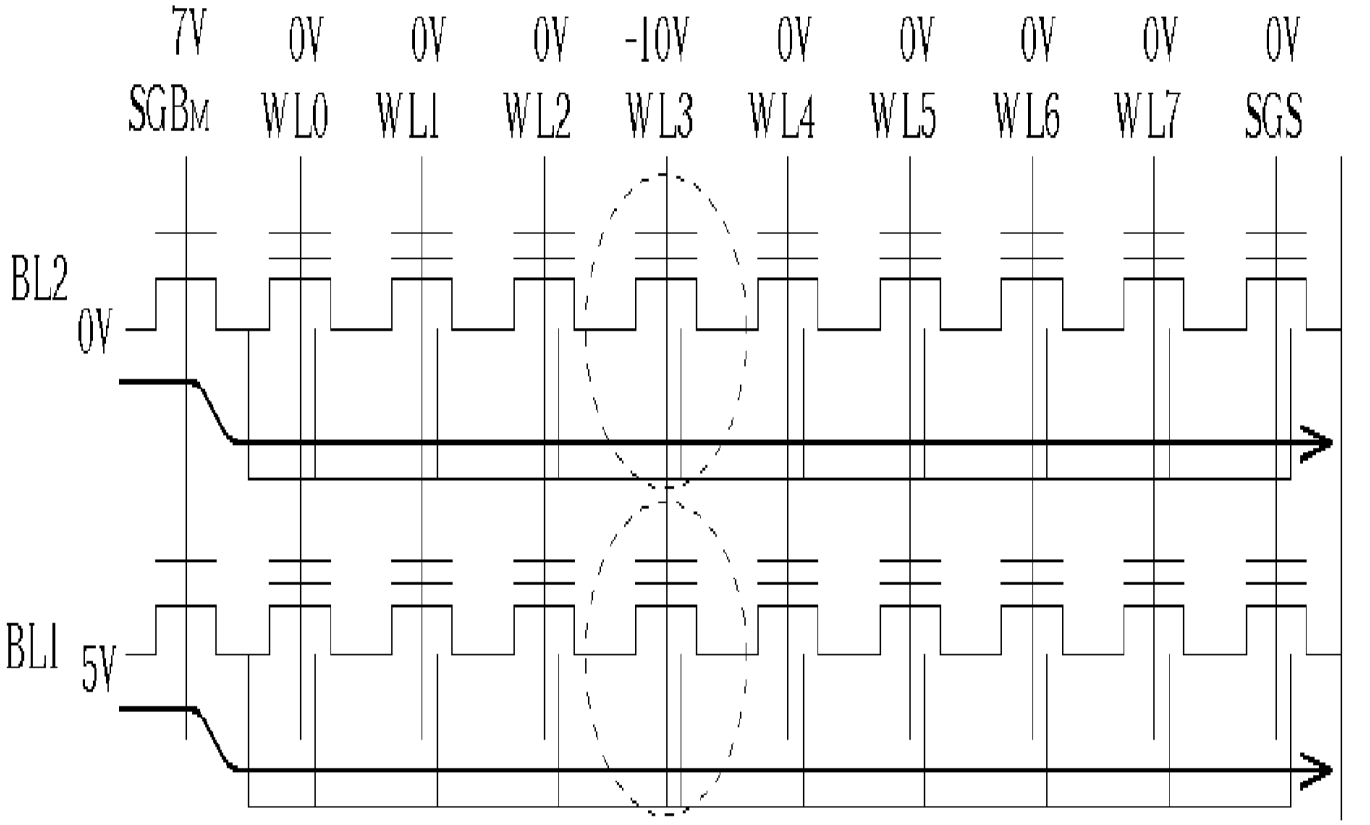


Fig. 5 (b)

READ OPERATION

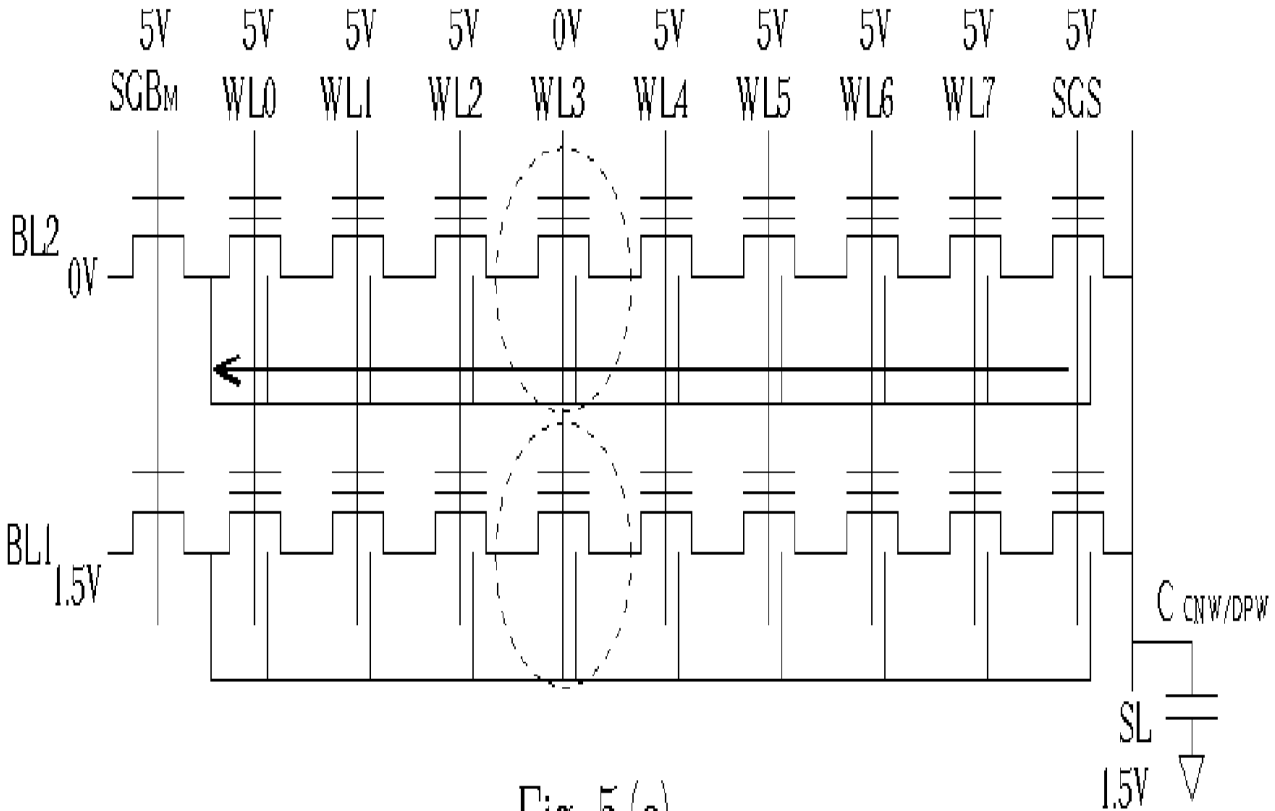


Fig. 5 (c)

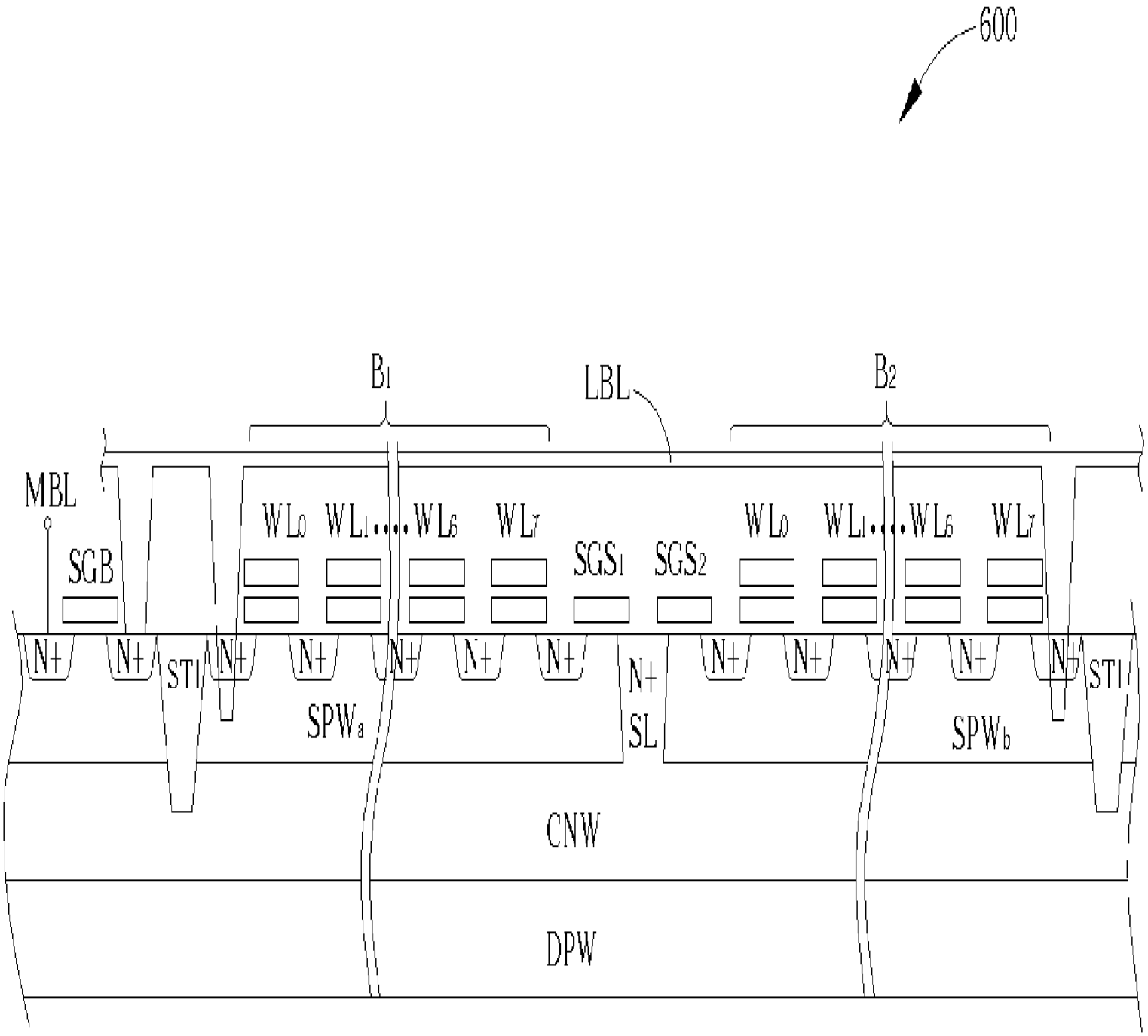
600
B1
LBL
B2
MBL
SGB
WL0
WL1
WL6
WL7
SGS1
SGS2
WL0
WL1
WL6
WL7
N+
STI
SPWa
SL
SPWb
CNW
DPW

Fig. 6

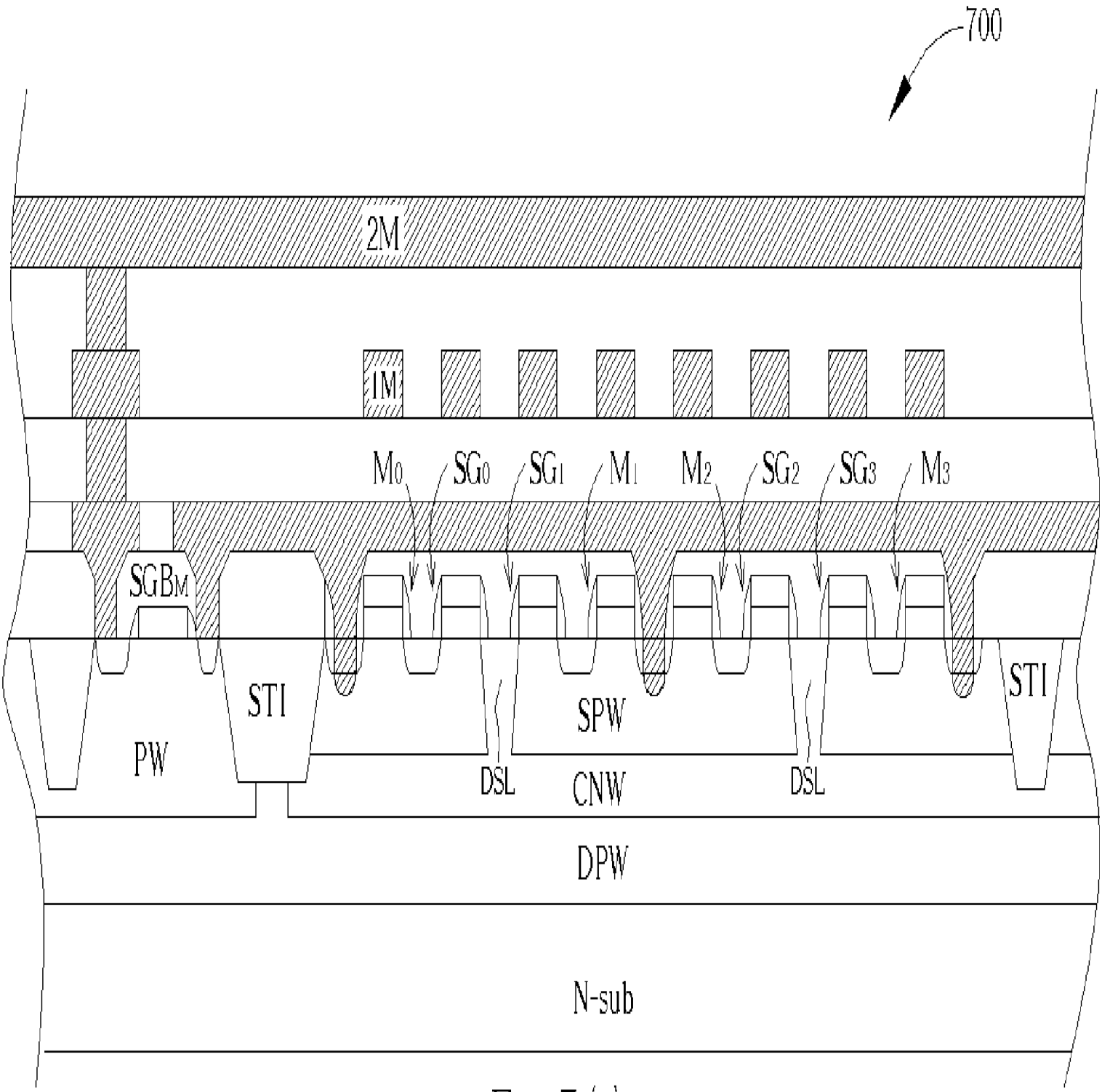
700
2M
1M
M0
SG0
SG1
M1
M2
SG2
SG3
M3
SGBM
STI
STI
PW
SPW
DSL
DSL
CNW
DPW
N-sub

Fig. 7 (a)

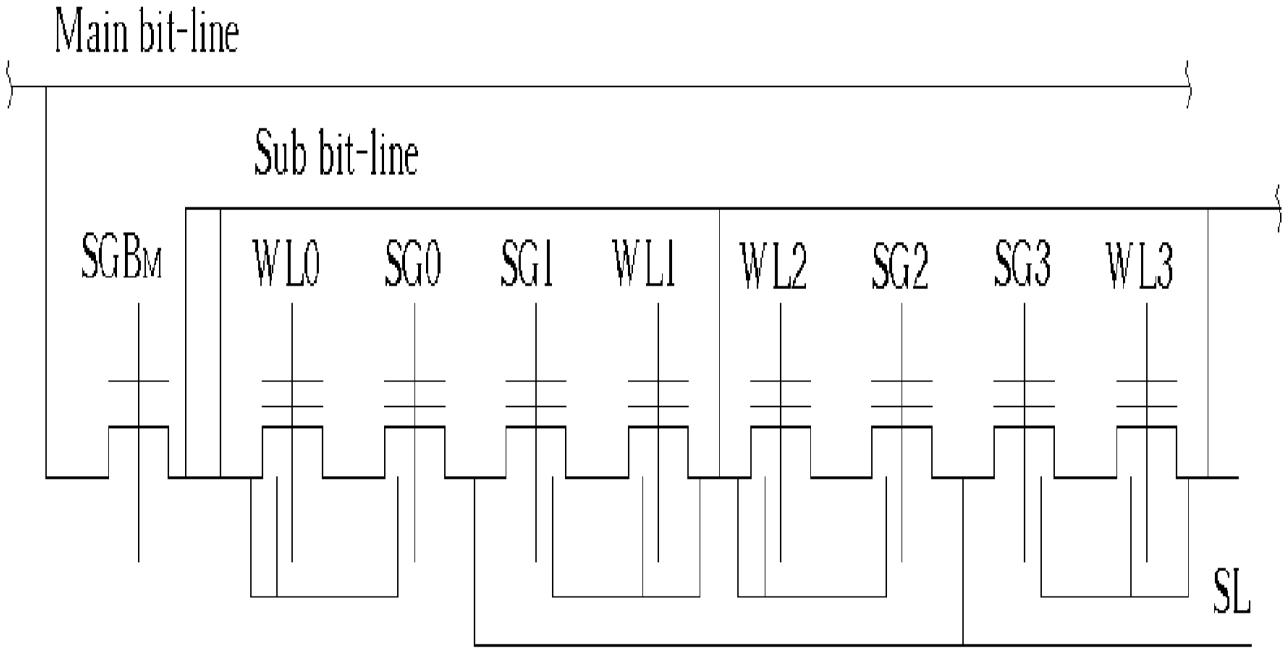
Main bit-line
Sub bit-line
SGBM
WL0
SG0
SG1
WL1
WL2
SG2
SG3
WL3
SL

Fig. 7 (b)

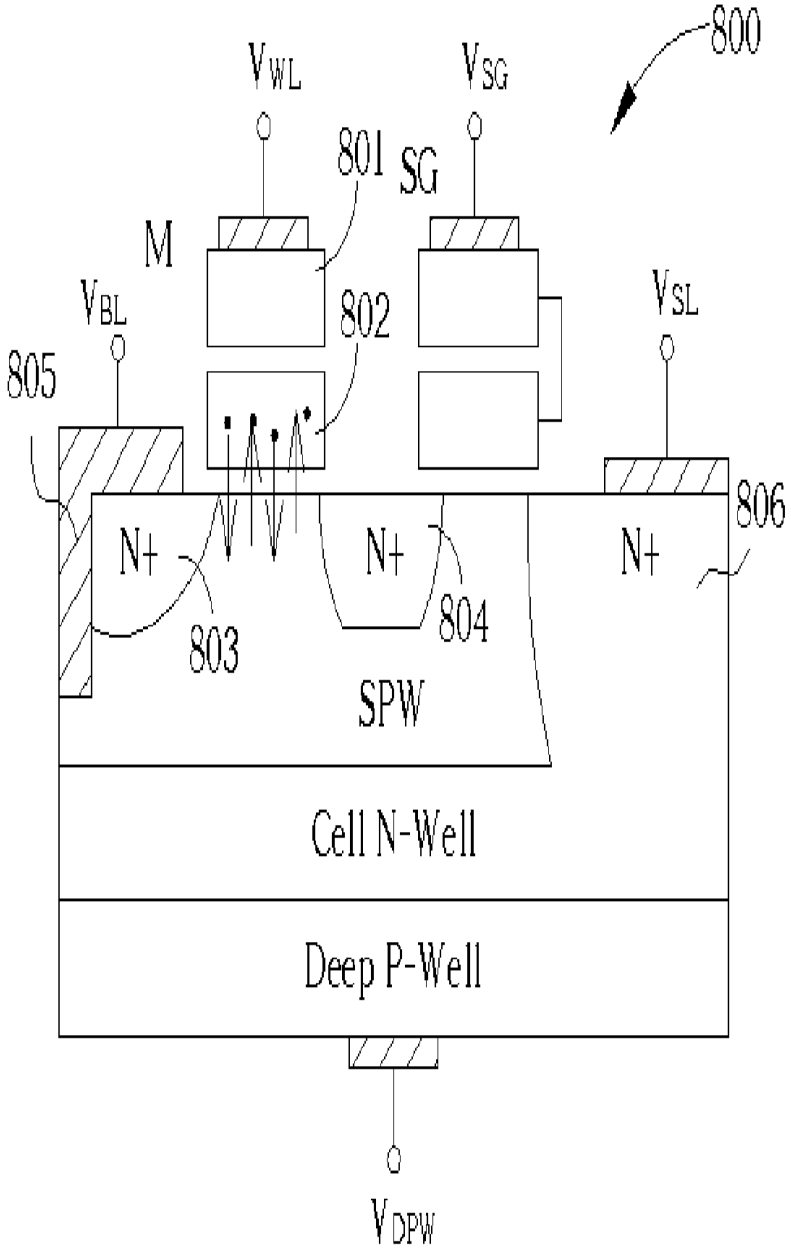
800
$V_{WL}$
$V_{SG}$
801
SG
M
$V_{BL}$
802
$V_{SL}$
805
806
N+
N+
N+
803
804
SPW
Cell N-Well
Deep P-Well
$V_{DPW}$

Fig. 8 (a)

| | $V_{BL}$ | $V_{WL}$ | $V_{SG}$ | $V_{SL}$ | $V_{DPW}$ |
|---|---|---|---|---|---|
| Program | 5V | -10V | 0V | Float | 0V |
| Erase | Float | 10V | -6V | -8V | -8V |
| Read | 0V | 0V | 5V | 1.5V | 0V |

Fig. 8 (b)

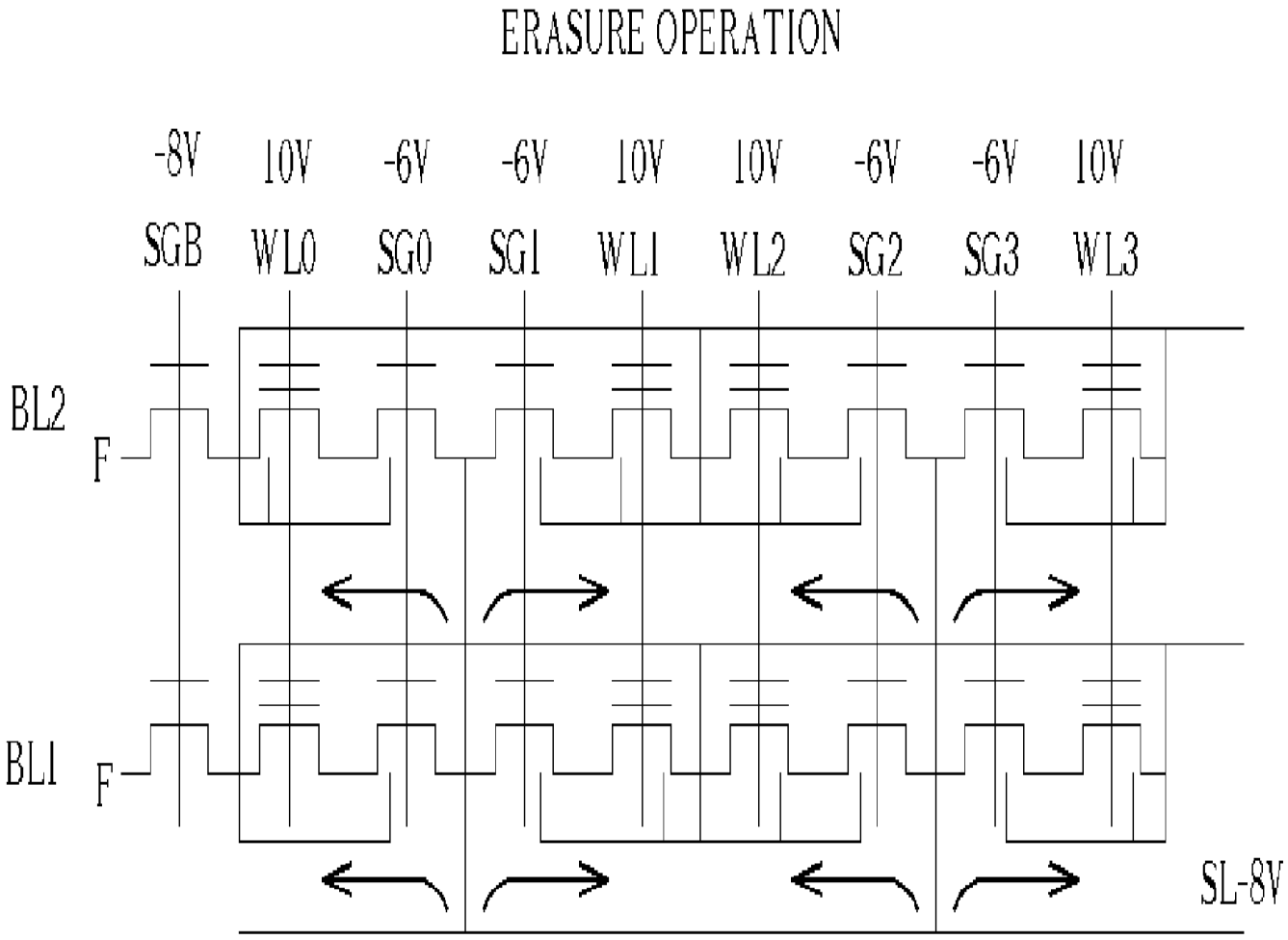
ERASURE OPERATION
-8V
10V
-6V
-6V
10V
10V
-6V
-6V
10V
SGB
WL0
SG0
SG1
WL1
WL2
SG2
SG3
WL3
BL2
F
BL1
F
SL-8V

Fig. 9 (a)

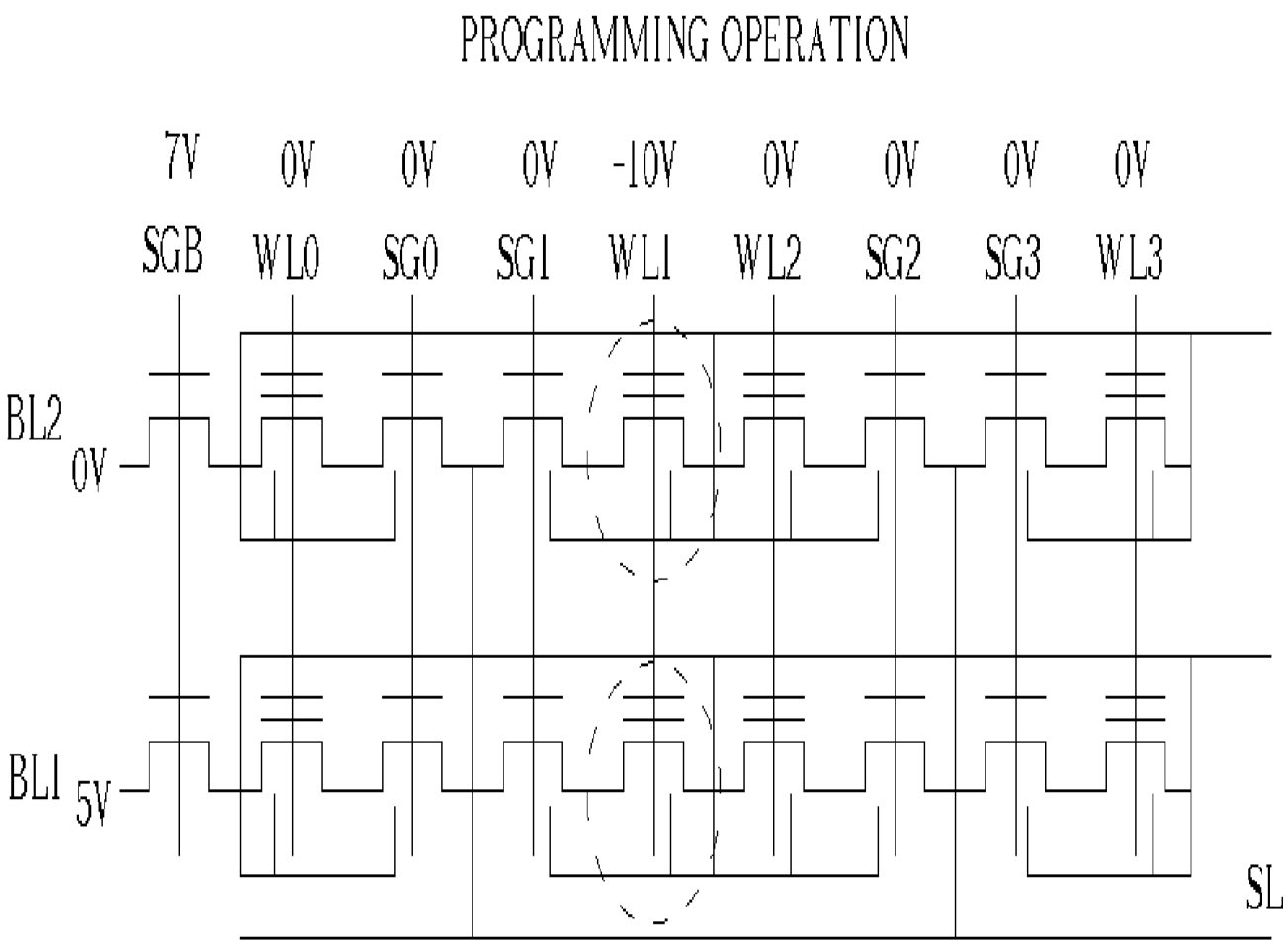
PROGRAMMING OPERATION
7V
0V
0V
0V
-10V
0V
0V
0V
0V
SGB
WL0
SG0
SG1
WLI
WL2
SG2
SG3
WL3
BL2
0V
BLI
5V
SL

Fig. 9 (b)

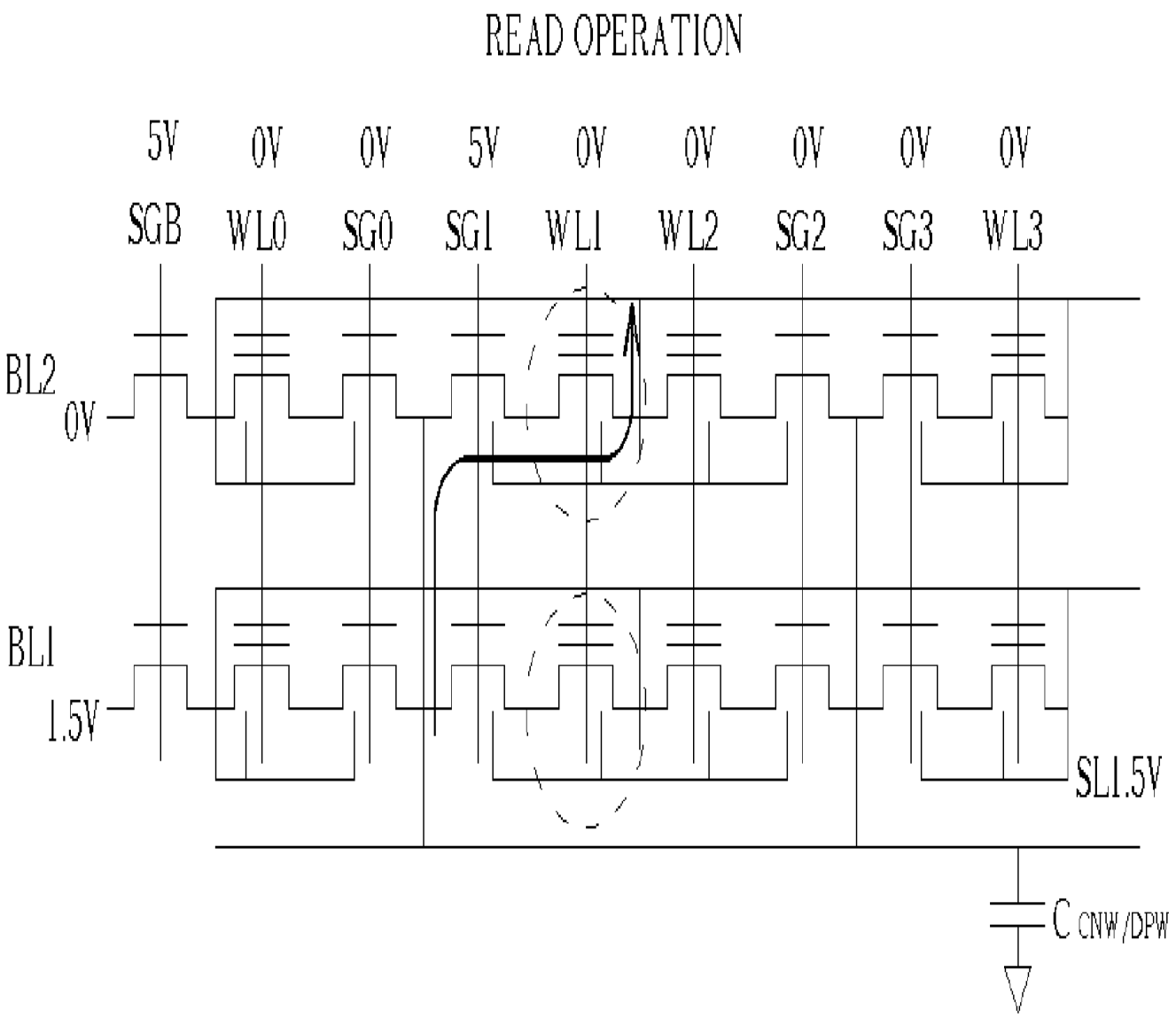
READ OPERATION
5V
0V
0V
5V
0V
0V
0V
0V
0V
SGB
WL0
SG0
SG1
WL1
WL2
SG2
SG3
WL3
BL2
0V
BL1
1.5V
SL1.5V
C CNW/DPW

Fig. 9 (c)

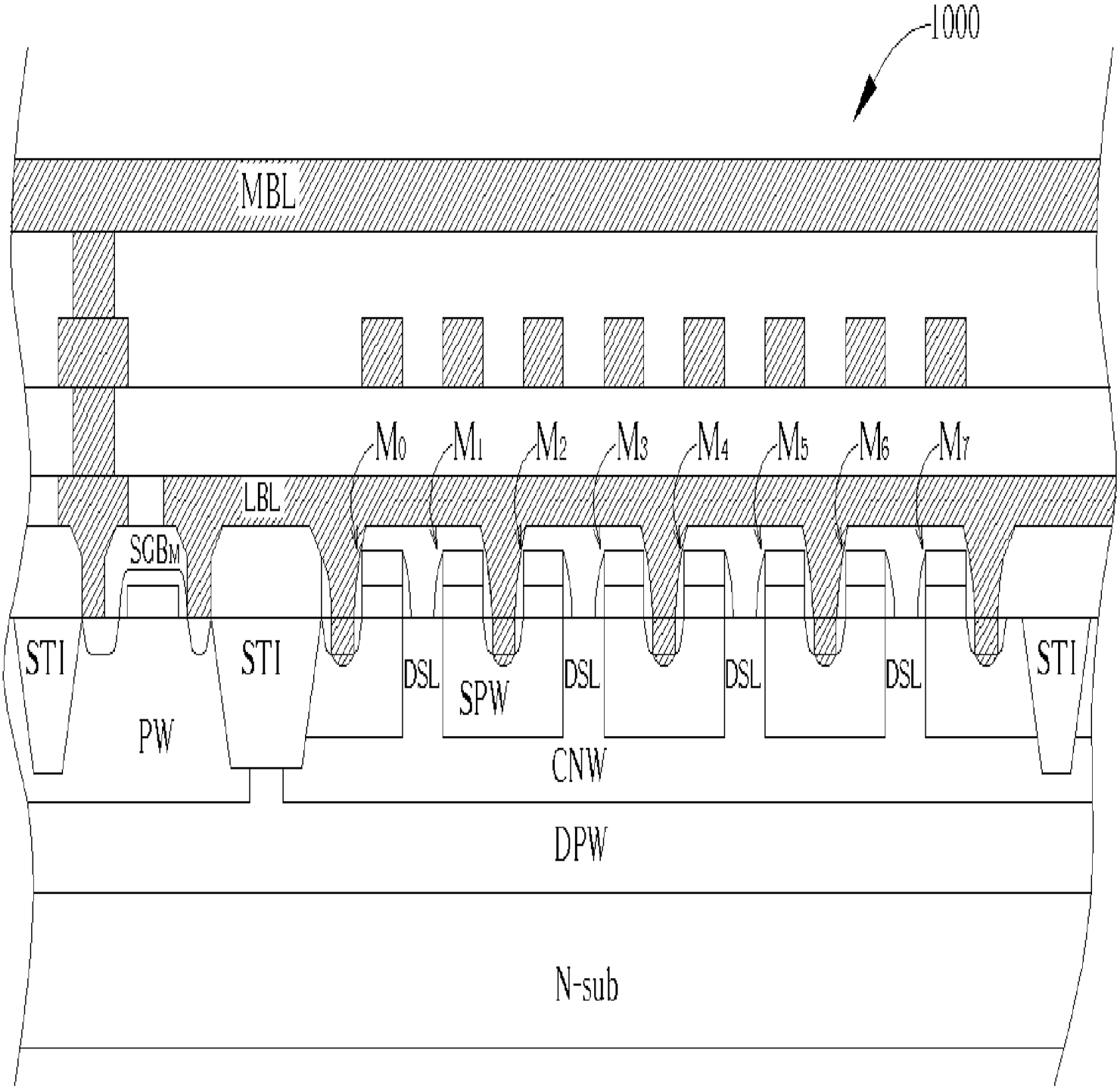
1000
MBL
M0
M1
M2
M3
M4
M5
M6
M7
LBL
SGBM
STI
STI
DSL
SPW
DSL
DSL
DSL
STI
PW
CNW
DPW
N-sub

Fig. 10 (a)

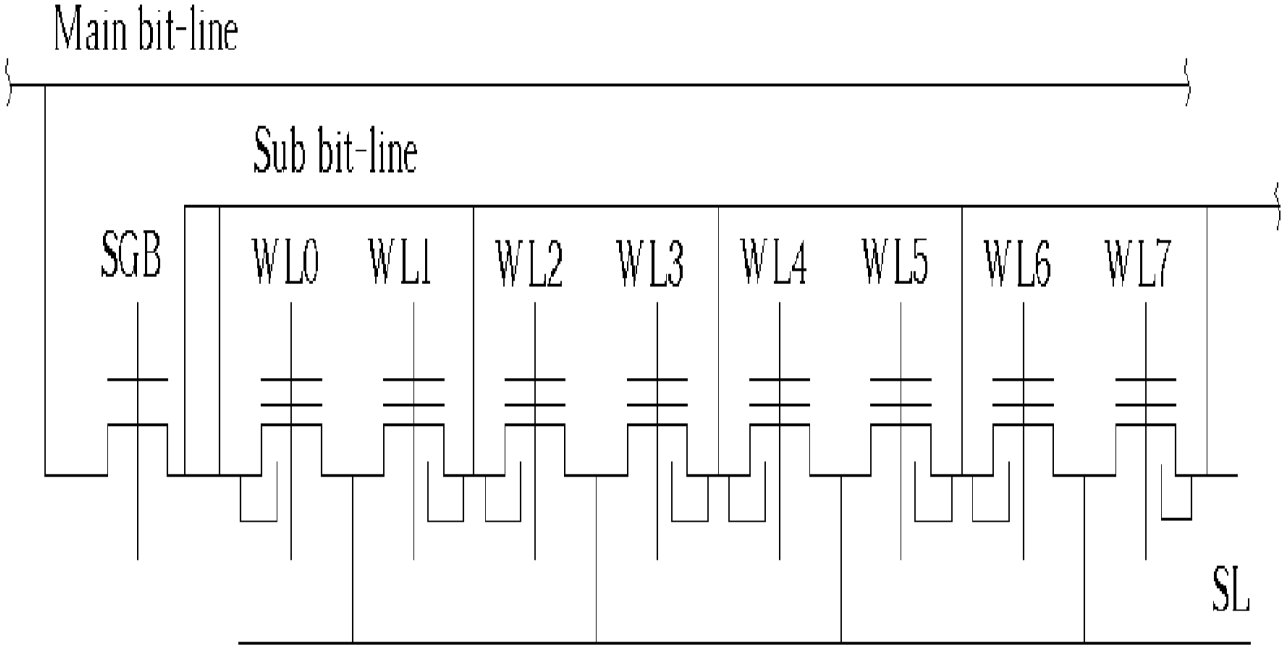
Main bit-line
Sub bit-line
SGB
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
SL

Fig. 10 (b)

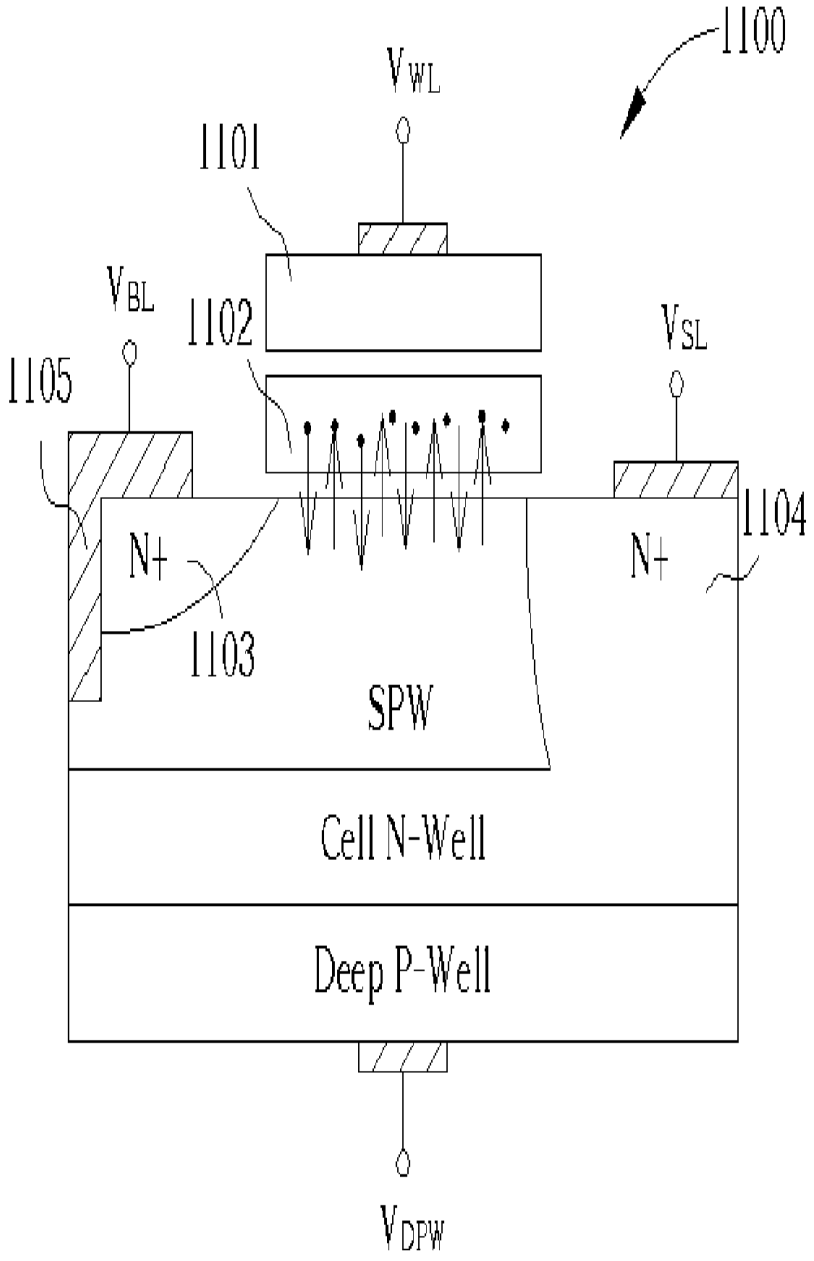
1100
$V_{WL}$
1101
$V_{BL}$
1102
$V_{SL}$
1105
1104
N+
N+
1103
SPW
Cell N-Well
Deep P-Well
$V_{DPW}$

Fig. 11 (a)

| | $V_{BL}$ | $V_{WL}$ | $V_{SL}$ | $V_{DPW}$ |
|---|---|---|---|---|
| Program | 5V | -10V | Float | 0V |
| Erase | Float | 10V | -8V | -8V |
| Read | 0V | 4V | 1.5V | 0V |

Fig. 11 (b)

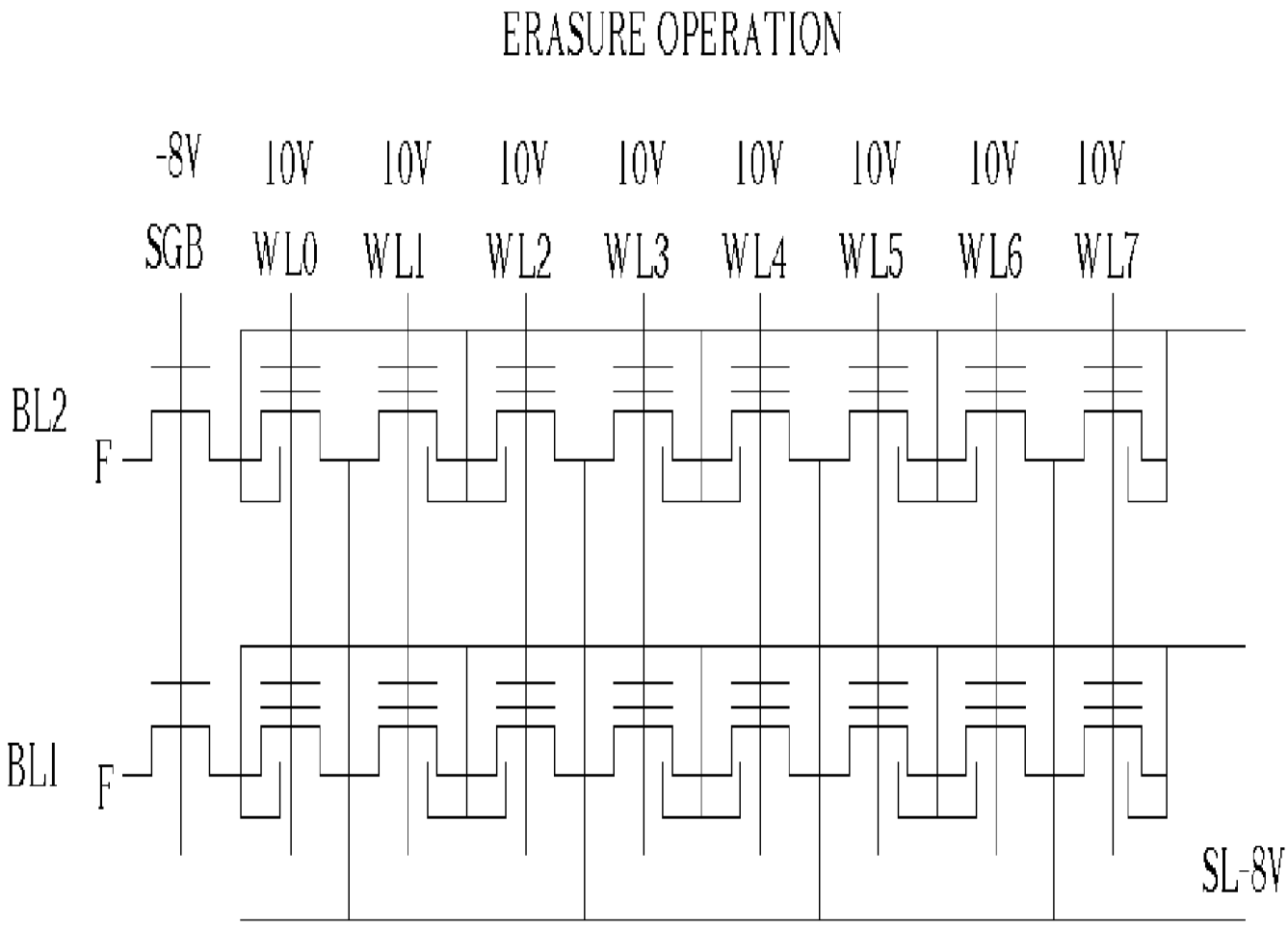
ERASURE OPERATION
-8V
10V
10V
10V
10V
10V
10V
10V
10V
SGB
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
BL2
F
BL1
F
SL-8V

Fig. 12 (a)

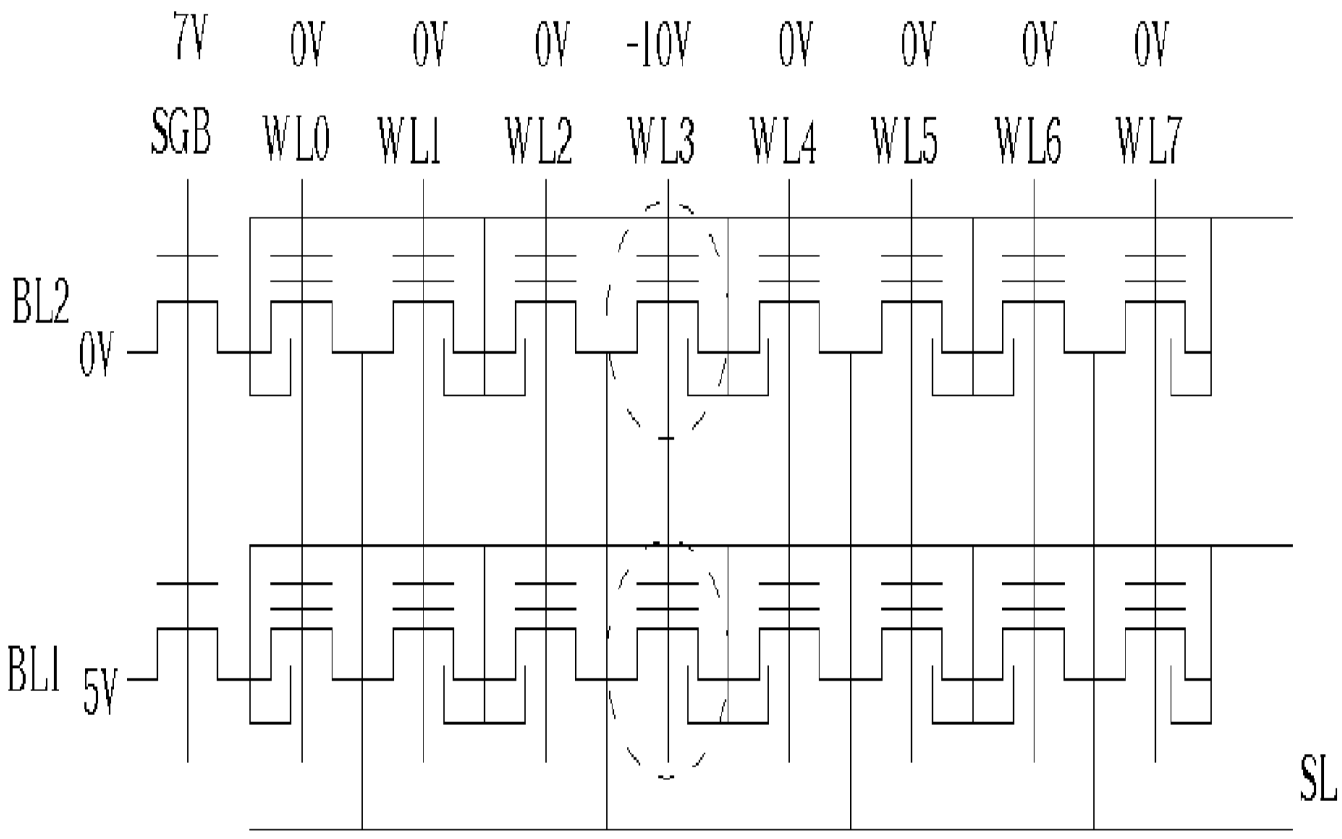
PROGRAMMING OPERATION
7V
0V
0V
0V
-10V
0V
0V
0V
0V
SGB
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
BL2
0V
BL1
5V
SL

Fig. 12 (b)

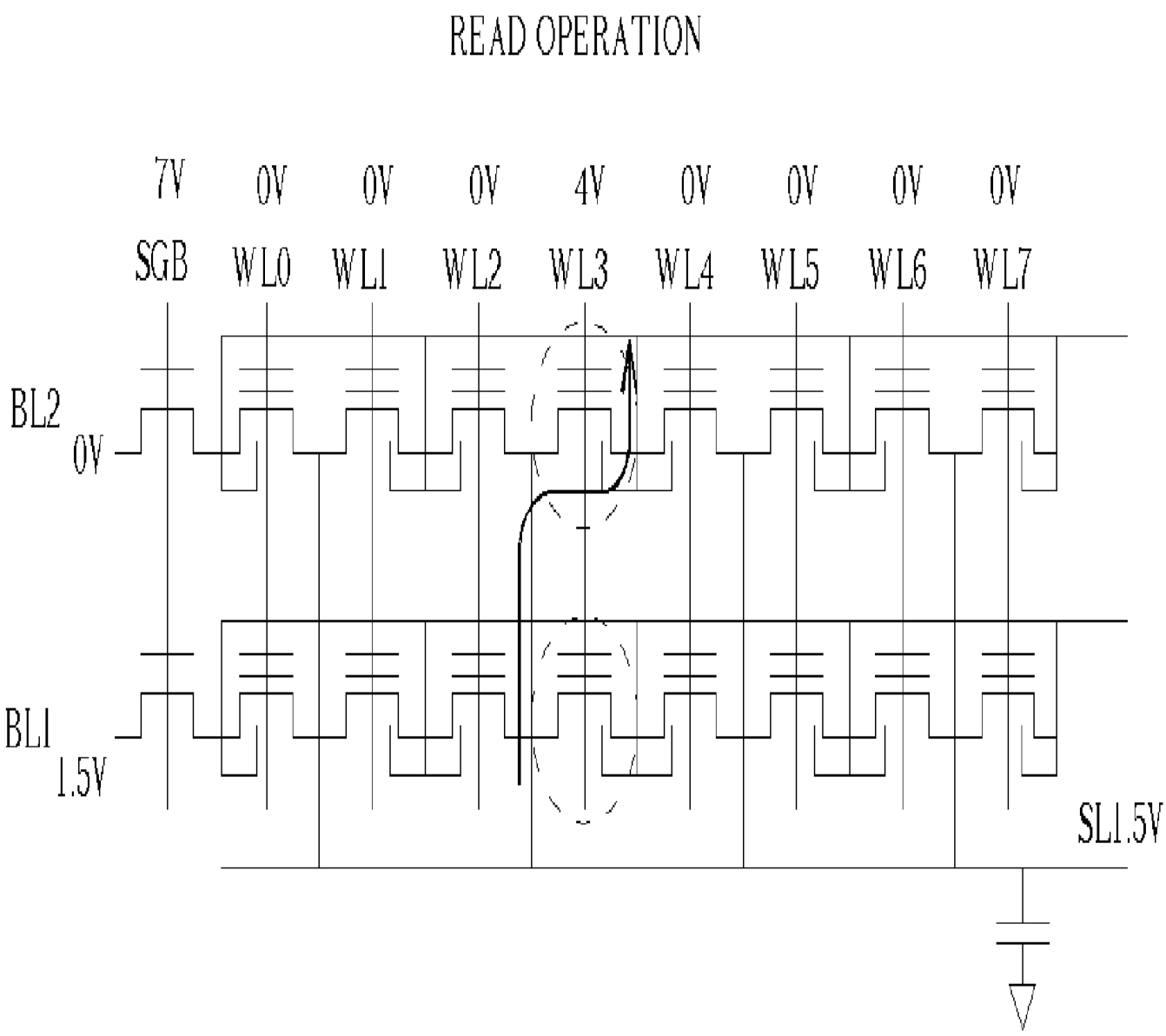
READ OPERATION
7V
0V
0V
0V
4V
0V
0V
0V
0V
SGB
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
BL2
0V
BL1
1.5V
SL1.5V

Fig. 12 (c)

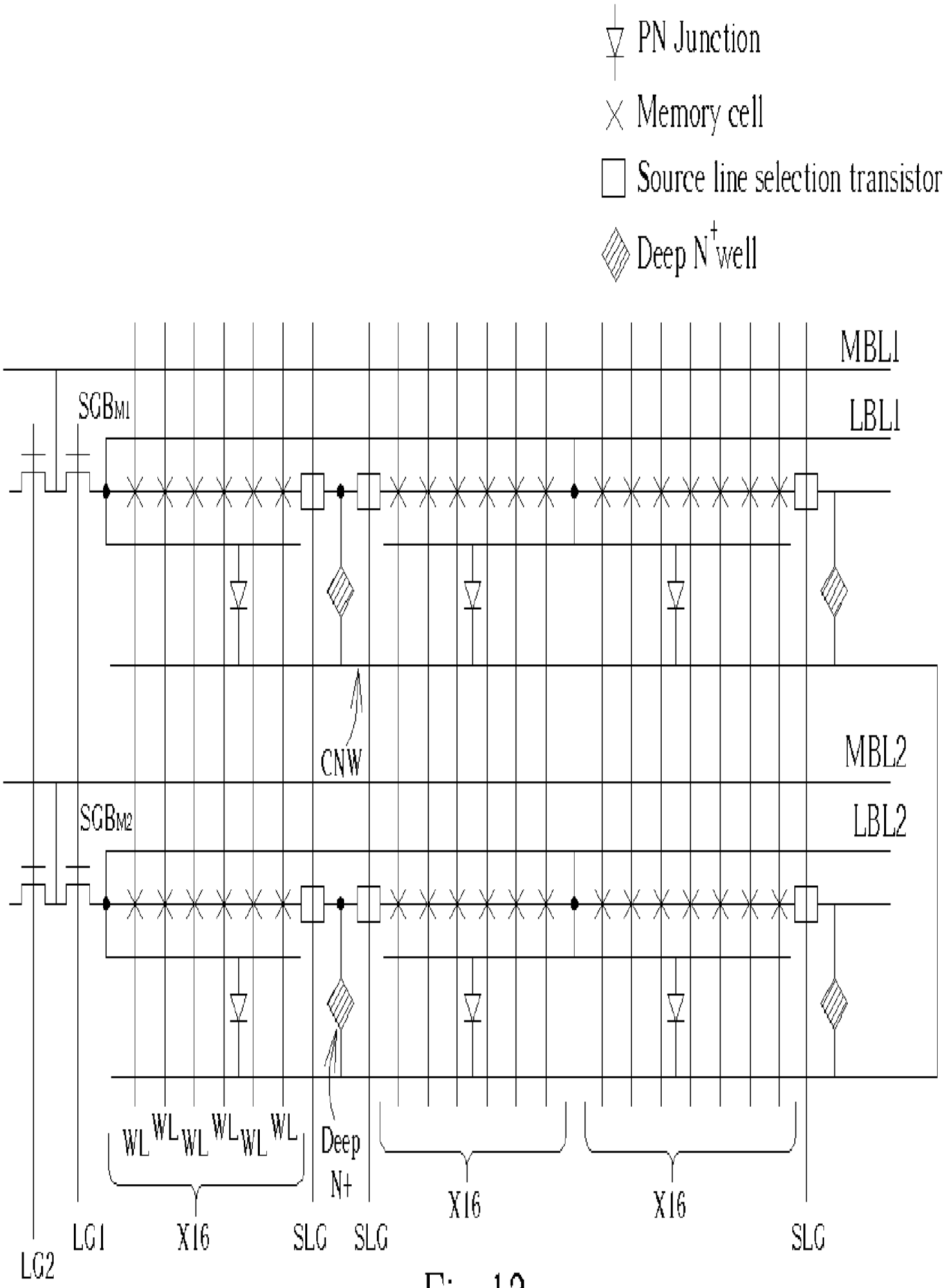
PN Junction
Memory cell
Source line selection transistor
Deep N+well
MBL1
LBL1
SGBM1
CNW
MBL2
LBL2
SGBM2
WL WL WL WL WL WL
Deep N+
X16
X16
X16
LG2
LG1
SLG
SLG
SLG

Fig. 13

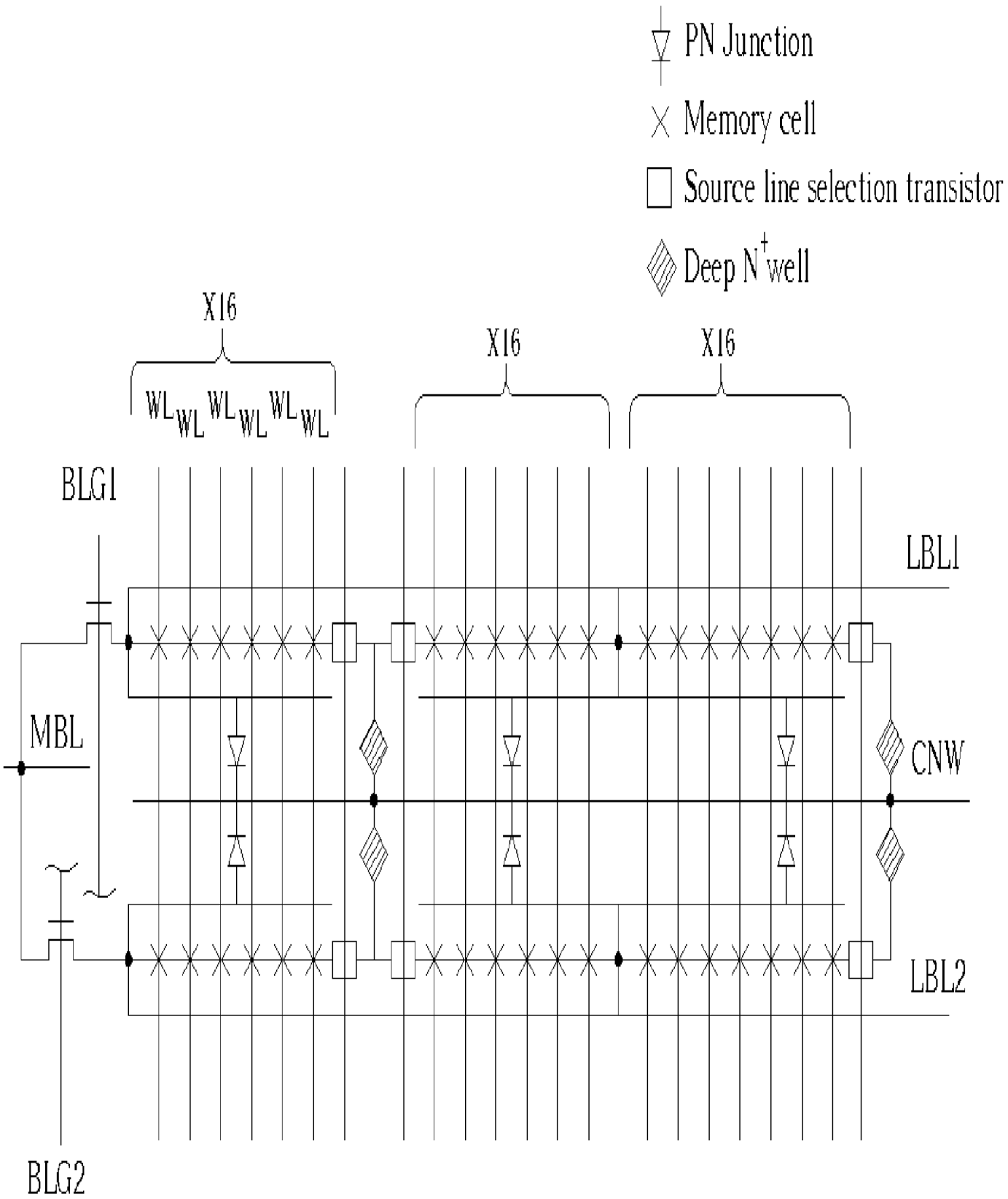
PN Junction
Memory cell
Source line selection transistor
Deep N+well
X16
X16
X16
WL WL WL WL WL
BLG1
LBL1
MBL
CNW
LBL2
BLG2

Fig. 14

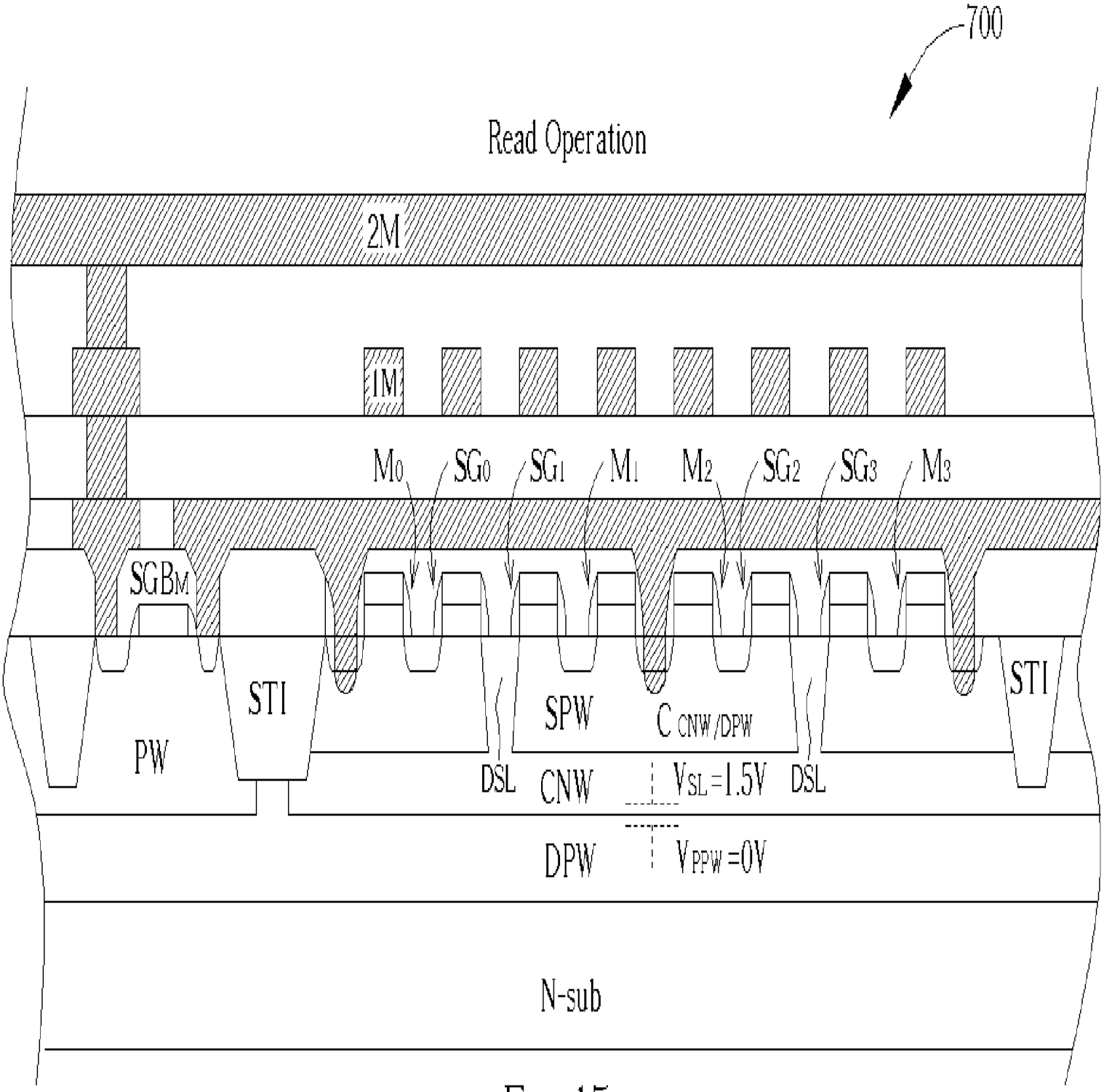
700
Read Operation
2M
1M
M0
SG0
SG1
M1
M2
SG2
SG3
M3
SGBM
STI
PW
SPW
C CNW/DPW
DSL
CNW
VSL=1.5V
DSL
STI
DPW
VPPW=0V
N-sub

Fig. 15